

IN THE CLAIMS

Please amend the claims as follows.

1. (Previously Presented) A process comprising:
forming a first recess in a substrate;
forming a conductive structure in the first recess having substantially vertical sidewalls;
first wet etching to expose a first portion of the conductive structure;
first rinsing the conductive structure; and
second non-wet etching to expose a second portion of the conductive structure.
2. (Original) The process of claim 1, wherein first wet etching includes first etching a polysilicon sacrificial second film that is disposed over the substrate.
3. (Original) The process of claim 1, and wherein first wet etching is at a rate that is faster than second non-wet etching.
4. (Currently Amended) The process of claim 1, A process comprising:
forming a first recess in a substrate;
forming a conductive structure in the first recess;
first etching to expose a first portion of the conductive structure;
first rinsing the conductive structure; and
second etching to expose a second portion of the conductive structure
wherein first wet etching is selected from the group consisting of a wet process and a vapor process, and wherein second non-wet etching is selected from the group consisting of a vapor process and a dry process.
5. (Previously Presented) The process of claim 1, wherein the substrate includes a single dielectric stack, wherein first wet etching is selected from the group consisting of a wet process and a vapor process, wherein second non-wet etching is selected from the group consisting of a vapor process and a dry process, and wherein the single dielectric stack is selected from the

group consisting of undoped spin-on dielectric, undoped vapor-deposited dielectric, doped spin-on dielectric, and doped vapor-deposited dielectric.

6. (Previously Presented) The process of claim 1, wherein the substrate includes a single dielectric stack, wherein first wet etching is selected from the group consisting of a wet process and a vapor process, wherein second non-wet etching is selected from the group consisting of a vapor process and a dry process, and wherein the single dielectric stack is selected from the group consisting of spin-on undoped silica, spin-on doped silica, borophospho silicate glass, borosilicate glass, phospho silicate glass, doped oxide from the decomposition of tetraethyl ortho silicate, and undoped oxide from the decomposition of tetraethyl ortho silicate.

7. (Canceled)

8. (Original) The process of claim 1, wherein forming a first recess includes forming the recess in a dielectric first film that is disposed above the substrate, and in a sacrificial second film that is disposed above and on the dielectric first film.

9. (Previously Presented) A process comprising:

forming a first recess in a substrate and wherein the first recess penetrates a dielectric first film that is disposed above the substrate and a sacrificial second film that is disposed above and on the dielectric first film;

forming a conductive structure in the first recess having substantially vertical sidewalls; first etching to expose a first portion of the conductive structure, wherein first etching includes a first etch chemistry;

rinsing the conductive structure; and

second etching to expose a second portion of the conductive structure, wherein second etching includes a second etch chemistry.

10. (Previously Presented) The process of claim 9, wherein first etching includes plasma etching of the sacrificial film, wherein the sacrificial film includes polysilicon selected from the group consisting of undoped polysilicon, and heavily doped polysilicon.
11. (Previously Presented) The process of claim 9, wherein first etching includes first etching the sacrificial second film, and wherein second etching includes second etching the dielectric first film, wherein the dielectric first film is selected from the group consisting of an undoped dielectric, a doped dielectric, a spin-on deposited dielectric, a vapor-deposited dielectric, an undoped polysilicon, a doped polysilicon, and combinations thereof, and wherein the sacrificial second film includes an undoped oxide.
12. (Original) The process of claim 9, wherein first etching removes the dielectric first film at a rate that is faster than second etching removes the sacrificial second film.
13. (Original) The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is vapor deposited.
14. (Original) The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is spin-on deposited.
15. (Original) The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is spin-on processed, and wherein the sacrificial second film is spin-on processed.
16. (Original) The process of claim 9, wherein the dielectric first film includes an undoped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is vapor deposited.

17. (Previously Presented) The process of claim 9, wherein the dielectric first film includes an undoped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is spin-on deposited.
18. (Original) The process of claim 9, wherein the dielectric first film includes an undoped oxide, wherein the sacrificial second film includes an undoped oxide, wherein the dielectric first film is spin-on deposited, and wherein the sacrificial second film is spin-on deposited.
19. (Original) The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes a doped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is vapor deposited.
20. (Original) The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes a doped oxide, wherein the dielectric first film is vapor deposited, and wherein the sacrificial second film is spin-on deposited.
21. (Original) The process of claim 9, wherein the dielectric first film includes a doped oxide, wherein the sacrificial second film includes a doped oxide, wherein the dielectric first film is spin-on deposited, and wherein the sacrificial second film is spin-on deposited.
22. (Original) A process comprising:
first etching a sacrificial second film to expose a first portion of a conductive structure, wherein first etching includes a first etch chemistry, and wherein first etching includes a first etch rate;
rinsing the conductive structure; and
second etching an amorphous carbon first film to expose a second portion of the conductive structure, wherein second etching includes a second etch chemistry, and wherein second etching includes a second etch rate that is slower than the first etch rate.

23. (Original) The process of claim 22, and wherein first etching removes the sacrificial second film at a rate that is faster than second etching removes the amorphous carbon first film.
24. (Original) The process of claim 22, wherein the sacrificial second film includes a doped oxide, and wherein the sacrificial second film is vapor deposited.
25. (Original) The process of claim 22, wherein the sacrificial second film includes a doped oxide, and wherein the sacrificial second film is spin-on processed.
26. (Original) The process of claim 22, wherein the sacrificial second film includes an undoped oxide, and wherein the sacrificial second film is vapor deposited.
27. (Original) The process of claim 22, wherein the sacrificial second film includes an undoped oxide, and wherein the sacrificial second film is spin-on processed.
28. (Previously Presented) The process of claim 22, wherein the sacrificial second film is selected from an oxide and a polysilicon, wherein first etching is selected from the group consisting of wet etching and vapor etching, and wherein second etching includes oxygen plasma stripping.
29. (Original) A process comprising:
 - first etching a sacrificial second film to expose a first portion of a conductive structure, wherein first etching includes a first etch chemistry;
 - first rinsing the conductive structure; and
 - second etching a dielectric first film, which is disposed below the sacrificial second film, to expose a second portion of the conductive structure, wherein second etching includes a second etch chemistry, and wherein first etching removes the sacrificial second film at a rate that is faster than second etching removes the dielectric first film.

30. (Original) The process of claim 29, wherein the dielectric first film includes an undoped oxide, and wherein first etching the sacrificial second film includes etching an undoped oxide.

31. (Original) The process of claim 29, wherein the dielectric first film includes an undoped oxide, and wherein first etching the sacrificial second film includes etching a doped oxide.

32. (Original) The process of claim 29, wherein the dielectric first film includes a doped oxide, and wherein first etching the sacrificial second film includes etching a doped oxide.

33. (Original) The process of claim 29, wherein the dielectric first film includes a doped oxide, and wherein first etching the sacrificial second film includes etching an undoped oxide.

34. (Original) The process of claim 29, wherein the dielectric first film includes an undoped oxide, and wherein first etching the sacrificial second film includes etching a doped polysilicon.

35. (Original) The process of claim 29, wherein the dielectric first film includes an undoped oxide, and wherein first etching the sacrificial second film includes etching an undoped polysilicon.

36. (Original) The process of claim 29, wherein the dielectric first film includes a doped oxide, and wherein first etching the sacrificial second film includes etching a doped polysilicon.

37. (Original) The process of claim 29, wherein the dielectric first film includes a doped oxide, and wherein first etching the sacrificial second film includes etching an undoped polysilicon.

38. (Original) The process of claim 29, wherein the dielectric first film includes an undoped polysilicon, and wherein first etching the sacrificial second film includes etching a doped polysilicon.

39. (Original) The process of claim 29, wherein the dielectric first film includes a lightly doped polysilicon, and wherein first etching the sacrificial second film includes etching a heavier-doped polysilicon.

40. (Previously Presented) A process comprising:
stripping amorphous carbon from a conductive structure embedded therein having substantially vertical sidewalls, wherein the conductive structure is coupled to a substrate active area, and wherein the conductive structure includes an aspect ratio from about 6:1 to about 25:1.

41. (Original) The process of claim 40, wherein the conductive structure includes a container capacitor, and wherein stripping includes oxygen plasma stripping.

42. (Original) The process of claim 40, wherein the conductive structure is embedded in at least one additional sacrificial film, including a TEOS-decomposed sacrificial second film that is disposed above and on the amorphous carbon as a first film.

43. (Original) The process of claim 40, wherein the conductive structure is embedded in at least one additional sacrificial film, wherein the at least one additional sacrificial film includes a BPSG sacrificial second film disposed above and on the amorphous carbon as a first film.

44. (Original) The process of claim 40, wherein the conductive structure is embedded in at least one additional sacrificial film wherein the at least one additional sacrificial film includes an oxide sacrificial second film disposed above the amorphous carbon as a first film.

45. (Original) The process of claim 40, wherein the conductive structure is embedded in at least one additional sacrificial film wherein the at least one additional sacrificial film includes a polysilicon sacrificial second film disposed above the amorphous carbon as a first film.

46. (Previously Presented) A process comprising:
 - forming a recess in a first dielectric stack;
 - forming a conductive structure in the recess, wherein the conductive structure has substantially vertical sidewalls, is partially embedded in the recess, and wherein the conductive structure is formed to extend from the first dielectric stack; and
 - electrically isolating the conductive structure.
47. (Original) The process of claim 46, the process further including:
 - forming a storage cell plate over the conductive structure.
48. (Original) The process of claim 46, wherein electrically isolating the conductive structure includes:
 - forming a storage cell dielectric film over the conductive structure.
49. (Original) The process of claim 46, the process further including:
 - forming a storage cell dielectric film over the conductive structure; and
 - forming a storage cell plate over the storage cell dielectric film.
50. (Original) The process of claim 46, wherein forming a storage cell dielectric film is carried out by chemical vapor deposition.

51-71. (Canceled)